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All You Need To Know About DisplayPort

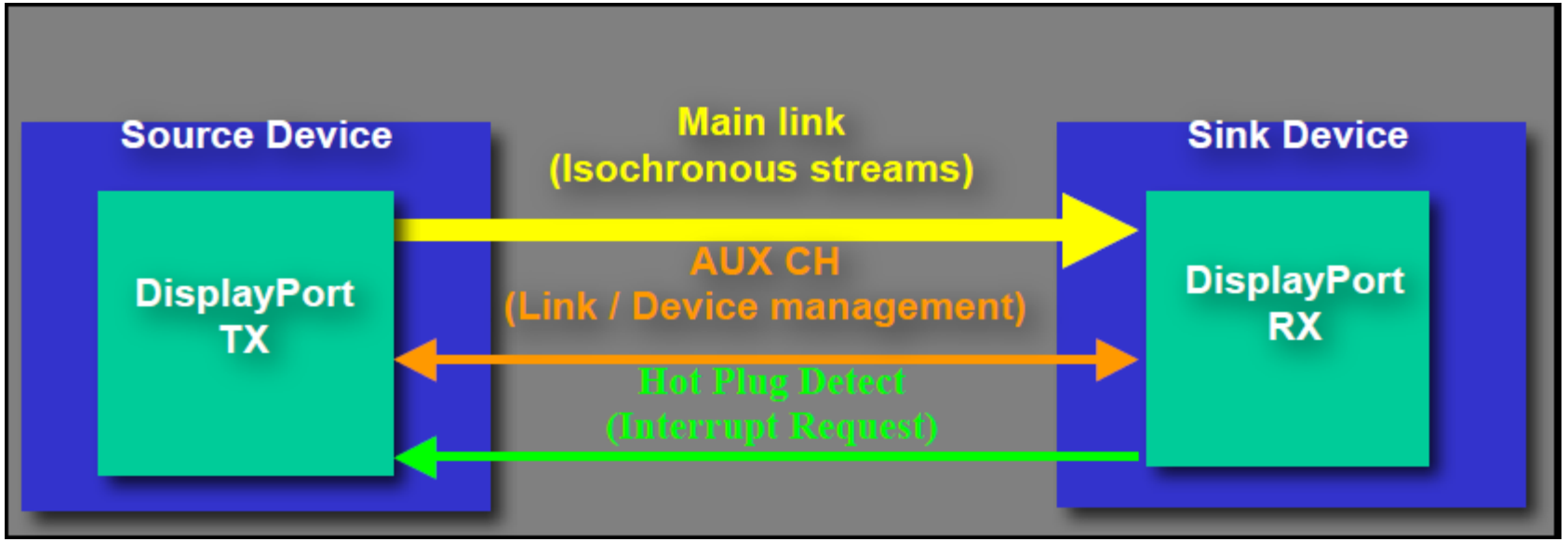
DisplayPort

What is DisplayPort?

- High-speed packet based interface
  - ✓ Enables multiple independent streams on a single cable
  - ✓ Can be combined with other standards such as USB and Thunderbolt
- Flexible lane configuration
  - ✓ Allows 1,2 or 4 lanes to be enabled depending on A/V stream requirements
  - ✓ DP Alt Mode in USB-C – 2 lanes for A/V stream and 2 lanes for USB 3.1
- Fixed rates can be selected
  - ✓ 1.62Gbps (RBR), 2.7Gbps (HBR), 5.4Gbps (HBR2), 8.1Gbps (HBR3) per lane
  - ✓ Up to 25.92 Gbps application bandwidth throughtput (at 4 lanes)
- Flexible pixel packing
  - ✓ Stream rate is decoupled from link rate
- NEW. HDCP 2.2
- NEW. FEC and DSC

DisplayPort Components

- Main Link
- Auxiliary channel (AUX CH)
- Hot Plug Detect (HPD)



Main Link

- 4 differential pairs (lane 0 to lane 3)
- Carries video & audio + their attributes (video parameters, audio format)
- 1,2 or 4 lanes in use
- All lanes used to carry video & audio
- Clock is synthesized at the Sink

Pixel data mapping over 4-lane Main

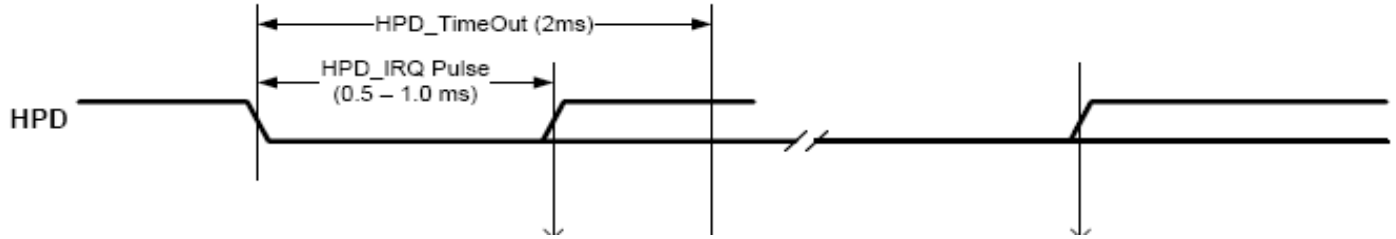
- Pixels 0, 4… : Lane 0,
- Pixels 1, 5… : Lane 1,
- Pixels 2, 6… : Lane 2,
- Pixels 3, 7… : Lane 3

AUX Channel

- Bidirectional, half-duplex, differential
- Carries link status and management data
- Source
  - ✓ Talks first
  - ✓ Places Requests
- Sink
  - ✓ Talks when requested
  - ✓ Places Replies
- Data transfer speed 1 Mbps

HPD (Hot Plug Detect)

- Pull-down at the Source side
- Set to 3 V (asserted) by the Sink to signal ”cable is plugged”
- Pulsed to GND by the Sink to request Source’s attention (interrupt request)
- HPD at GND for:
  - < 0.25 ms → glitch
  - 0.25 ms - 2 ms → interrupt request from Sink
  - > 2 ms → unplug



DP Sink Components

- DisplayPort Configuration Data (**DPCD**): a virtual memory with addresses 0x00000 – 0xFFFFF.
- Extended Display Identification Data (**EDID**): traditional (I^2C) serial memory.

AUX Channel Details

- Source Request + Sink Reply = Transaction
- Addressing a DPCD location →Native transact.
- Addressing a I²C device → I²C transact.
- Reply can be ACK, NACK or DEFER (= wait)

DPCD

DPCD Field	DPCD Addresses
Receiver Capability	00000h - 000FFh
Link Configuration	00100h - 001FFh
Link/Sink Device Status	00200h - 002FFh
Source Device-specific	00300h - 003FFh
Sink Device-specific	00400h - 004FFh
Branch Device-specific	00500h - 005FFh
Link/Sink Device Power Control	00600h - 006FFh
eDP-specific	00700h - 007FFh

DPCD

DPCD Field	DPCD Addresses
Sideband MSG Buffers	01000h - 017FFh
DPRX Event Status Indicator	02000h - 021FFh
Extended Receiver Capability	02200h - 022FFh
Protocol Converter Extension	03000h - 030FFh
Multi-touch (for eDP)	60000h - 61CFFh
HDCP 1.3 and HDCP2.2	68000h - 69FFFh
LT-tunable PHY Repeater	F0000h - F02FFh
MyDP-specific	FFF00h - FFFFFh

Link Training Procedure

1. A Sink is plugged (HPD = 3V)
2. Source reads the EDID
   (what video modes are supported?)
3. Source reads the DPCD
   (how many lanes, which bitrates are supported?)
4. Source decides how many lanes to use,
   the bitrate and starts Link Training
5. Sink reports about received signal quality and desired signal voltage and pre-emphasis
6. Source updates its PHY levels and iterates to step 5.

FEC Characteristics

- FEC (Forward Error Correction), new to DP standard 1.4
- Reed-Solomon code, RS(254,250)
  - ✓ FEC block 250 symbols + 4 RS parity symbols
  - ✓ +5 FEC parity code +1 CD_ADJ (disparity) code
  - ✓ 2.4% Overhead
  - ✓ Corrects 2 errors
  - ✓ Will work:
    - SST and MST mode
    - Uncompressed or DSC bitstream (required by standard to use FEC)

FEC DPCD registers

Register	DPCD Address
FEC_CAPABILITY (Sink sets)	0x00090
FEC_CONFIGURATION (Source sets)	0x00120
FEC_STATUS (Sink sets)	0x00280
FEC_ERROR_COUNT (Sink sets)	0x00281 – 0x00282

Compression Requirements

- Compression required for higher resolution and framerate
- In USB-C Alt-mode DisplayPort BW may be halved
- VESA requirements:
  - ✓ Visually lossless
  - ✓ Independently decodable regions
  - ✓ Many color formats and bit depths
  - ✓ Easy and inexpensive implementation in realtime
- MPEG-2, H.264, JPEG-2000 and VC-2
  - ✓ Require storage of many lines => expensive
- JPEG-LS:
  - ✓ Cannot guarantee constant bit rate
  - ✓ Quality not good enough when lossy

DSC Characteristics

- DSC (Display Stream Compression) new to DP standard 1.4
- Real time, frame-by-frame
- Image can be split to slices
- 3 pixels per clock (4:4:4)
- Typically 1:2 or 1:3 compression ratio, visually lossless
- v1.2a supports:
  - ✓ 4:4:4, 4:2:2, 4:2:0 color formats, RGB and YCbCr
  - ✓ 8-16 bits per color component
- Works as SST or MST
- VESA provides C-source code as example implementation

DSC Versions

Features	DSC 1.1	DSC 1.2a	VDC-M 1.1
Visually lossless compression performance verified by subjective testing			
30 bit color, compression ratio (bits/pixel)	3.75:1 (8 bpp)	3.75:1 (8 bpp)	5:1 (6 bpp)
24 bit color, compression ratio (bits/pixel)	3:1 (8 bpp)	3:1 (8 bpp)	4:1 (6 bpp)
IC complexity	Low	Low	Medium
Backwards compatibility	DSC 1.x	DSC 1.x	N/A
Both encoder and decoder are specified	✓	✓	✓
Normative C language code	✓	✓	✓
Frame-by-frame compression	✓	✓	✓
Bits per color support	8/10/12	8/10/12/14/16	8/10/12
High Dynamic Range-ready	✓	✓	✓
RGB and YCbCr 4:4:4 native encoding	✓	✓	✓
YCbCr 4:2:0 or 4:2:2 native encoding	No	✓	✓
Image test data base available from VESA	✓	✓	✓
Compliance test guideline and test scripts	✓	In development	
Publicly known adopting standards	MIPI DSI 1.2 DSI-2 1.0 VESA eDP 1.4b	HDMI 2.1 VESA DP 1.4a	MIPI DSI-2 1.1

✓ Available now

DSC DPCD registers

Register	DPCD Address
Receiver DSC Capabilities (Sink sets)	0x00060 – 0x0006F
DSC Enable (Source sets)	0x00160
DSC Status (Sink sets)	0x0020F

HDCP 2.2 CTS

- Transmitter Tests (UCD family certified by DCP LLC)
  - 1A test set – downstream procedure with Receiver
  - 1B test set – downstream procedure with Repeater
- Receiver Tests (UCD family certified by DCP LLC)
  - 2C test set – upstream procedure with Transmitter
- Repeater Tests (UCD-400 certification is in progress)
  - 3A test set – downstream procedure with Receiver
  - 3B test set – downstream procedure with Repeater
  - 3C test set – upstream procedure with Transmitter

DP 1.4 Link Layer CTS (under GMR at VESA)

- Source Device Tests
  4.2.1 – AUX reads after HPD Plug event
  4.2.2 – EDID and DPCD reads
  4.3.1 – Link Training
  4.3.2 – Link Maintenance
  4.3.3 – Video Time Stamp generation
- Sink Device Tests
  5.2.1 – AUX Channel Protocol
  5.2.2 – Sink Device DPCD Field Implementation
  5.3.1 – Link Training
  5.3.2 – Link Maintenance (development in progress)

Thank You!

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